PATENT ABSTRACTS OF JAPAN

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H01C 7/10

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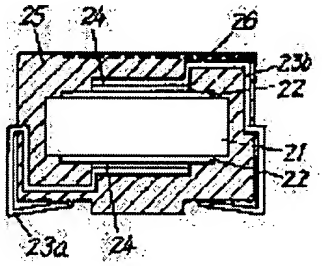
(72)Inventor : NAKAMURA KAZUYUKI
SATO MASAAKI

(54) CHIP-TYPE VARISTOR

(57)Abstract:
PROBLEM TO BE SOLVED: To enable a chip-type varistor to be surely kept in an open state when it is broken down by a method wherein a groove is provided to the upper surface of a molding resin along the outer circumference of a lead terminal.
SOLUTION: When an abnormal high voltage which a ceramic varistor device 21 is not able to withstand is applied to it, it is broken down. The varistor device 21 grows high in temperature, its composition is partially vaporized to produce gas of high pressure and temperature. The pressure of the gas acts on a molding resin 25 so as to break it, a fissure is opened along a groove 26, and the molding resin 25 is sheared off. The molding resin 25 on the upside of the ceramic varistor device 21 is separated off together with a lead terminal 23b by the pressure of gas just as a lid is opened, whereby the ceramic varistor device 21 is kept in an electrically opened state. By this setup, a chip-type varistor which is surely kept in an open state when it gets out of order can be obtained.



LEGAL STATUS

[Date of request for examination] 21.10.1999

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[Date of final disposal for application]	
[Patent number]	3381485
[Date of registration]	20.12.2002
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[Date of requesting appeal against examiner's decision of rejection]	
[Date of extinction of right]	

* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The chip mold varistor characterized by having had the resin mould of a varistor component, the electrode prepared in this principal plane, the lead terminal electrically connected to said electrode, and a said varistor component and electrode, and a lead terminal which covered the connection with an electrode at least, and establishing a slot in the up front face of mould resin along with said lead terminal periphery.
[Claim 2] The chip mold varistor according to claim 1 which gave spring nature to the lead terminal.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the chip mold varistor used for the cure against abnormal voltage which absorbs the surge voltage produced in power circuits, such as a television receiver, a washer, and automobile electrical equipment.
[0002]
[Description of the Prior Art] In drawing 15 and drawing 16 , 11 is a varistor component. They are a lead terminal and the electroconductive glue with which the electrode which prepared 12a and 12b in the principal plane of the varistor component 11, and 13a and 13b connect 14a, and 14b connects lead terminals 13a and 13b with Electrodes 12a and 12b. 15 is mould resin. About the chip mold varistor constituted as mentioned above, the actuation is explained below.
[0003] First, when the load of the abnormality high tension which varistor component 11 self cannot bear is carried out, the varistor component 11 causes penetration destruction.
[0004]
[Problem(s) to be Solved by the Invention] With the aforementioned conventional configuration, when it is covered with mould resin 15 and the varistor component 11 carries out penetration destruction, the high pressure gas which occurs in connection with it destroys mould resin 15, and the flow of the varistor component 11 and lead terminals 13a and 13b is severed. However, it had the problem that there was a possibility that the varistor component 11 may not be in an open condition depending on the part where mould resin 15 is destroyed.
[0005] When this invention solves the conventional technical problem and the varistor component 11 carries out penetration destruction, it aims at making it be in an open condition certainly.
[0006]
[Means for Solving the Problem] In order to attain this object, the chip mold varistor of this invention establishes a slot in the up front face of the mould resin in alignment with a lead terminal periphery, and, thereby, attains the early object.

[0007]
[Embodiment of the Invention] According to invention of this invention according to claim 1, it becomes weaker than a part without the mechanical-strength fang furrow of the part of the slot established in the up front face of mould resin. Therefore, when a varistor component causes penetration destruction, it is sheared from the part of a slot with the pressure of the gas which occurred, and the mould resin on the top face of a lead terminal exfoliates with a lead terminal so that a lid may open. For this reason, it will be in an open condition electrically between an electrode and a lead terminal.
[0008] (Operation gestalt 1) The plan of a chip mold varistor [in / in drawing 1 / the example of this invention] and drawing 2 show top-face perspective drawing, and drawing 3 shows the A-A sectional view of drawing 1 . In drawing 3 , 21 is the ceramic varistor component of a zinc oxide system. The electrode which prepared 22 in the principal plane of the ceramic varistor component 21, and 23a and 23b are lead terminals. 24 is electroconductive glue which connects lead terminals 23a and 23b with an electrode 22 electrically. The mould resin which consists of epoxy insulation resin with which 25 covered the whole varistor, and 26 are the slots established in the up front face of mould resin 25 along with the lead terminal 23b periphery. Actuation of the varistor constituted as mentioned above is explained using drawing.

[0009] Although the ceramic varistor component 21 is a good insulator in a steady state, if the abnormality high tension which ceramic varistor component 21 self cannot bear is impressed, the ceramic varistor component 21 will cause penetration destruction. Under the present circumstances, the destroyed ceramic varistor component 21 becomes an elevated temperature, and a part of presentation evaporates. An elevated temperature and high-pressure gas occur in connection with this. It works so that mould resin 25 may be destroyed, and along with the part of the weak slot 26 on the mechanical strength, with lead terminal 23b, the pressure of this gas produces a crack, and it exfoliates so that a lid may open [the mould resin 25 of ceramic varistor component 21 top face], and it is made to shear and it will be in an open condition electrically with the pressure of that gas. Mould resin 25 on top shows the condition of having exfoliated so that a lid might open to drawing 4 and drawing 5 , with lead terminal 23b in this operation gestalt. A side elevation is shown as well as the plan of the lead terminals 23a and 23b used for drawing 6 at this example, and drawing 7 . The resistance after penetration destruction of the chip mold varistor in this example and the resistance after penetration destruction of the chip mold varistor of the conventional example are shown as compared with (a table 1). In addition, an electrical potential difference twice the electrical potential difference of the maximum permissible is impressed to the ceramic varistor component 21, and overvoltage destruction is made to cause.

[0010]

[A table 1]

破壊後の端子間抵抗値Ω　n＝10		
従来品	実施形態１品	実施形態２品
22	300000以上	300000以上
73	2927	300000以上
209	300000以上	300000以上
3582	300000以上	300000以上
3	300000以上	300000以上
24	52000	300000以上
16	300000以上	300000以上
229	375	300000以上
2	526	300000以上
146	300000以上	300000以上

※抵抗測定器の測定範囲 300000Ω Max.

[0011] this (table 1) -- from -- as for the chip mold varistor by this invention, it turns out that the resistance after destruction will be in an open condition so that clearly. As mentioned above, this operation gestalt can establish a slot 26 in the up front face of mould resin 25 along with the periphery of lead terminal 23b, and can change the failure mode of the chip mold varistor at the time of the ceramic varistor component 21 carrying out penetration destruction into an open condition.

[0012] (Operation gestalt 2) In drawing 8 - drawing 10 , for an electrode, and 33a and 33b, as for electroconductive glue and 35, a lead terminal and 34 are [a ceramic varistor component and 32 / mould resin and 36] the slots on the front face of up of mould resin 35, and 31 is the same configuration as the operation gestalt 1. Differing from the operation gestalt 1 is the point of having given spring nature so that it might be easy to separate, when the ceramic varistor component 31 carried out penetration destruction at lead terminal 33b. The side elevation was shown as well as the plan of the lead terminals 33a and 33b used for drawing 13 at this example, and drawing 14 . Since bending is carried out to the include angle of 45 degrees from the middle of lead terminal 33b used for this example, this is pressed to the ceramic varistor component 31 side, and a wrap and spring nature are demonstrated by mould resin 35. Drawing 11 and drawing 12 show the state diagram which exfoliated so that a lid might open with lead terminal 33b along with the mould resin 35 fang furrow 36 of ceramic varistor component 31 electrode 32 top face, when the ceramic varistor component 31 in this operation gestalt carries out penetration destruction.

[0013] Actuation of the chip mold varistor constituted as mentioned above is explained using drawing. The include angle which lead terminal 33b which exfoliated with the pressure of gas opens since lead terminal 33b used for this

operation gestalt 2 although the process until lead terminal 33b shears mould resin 35 by penetration destruction of the ceramic varistor component 31 is the same as the operation gestalt 1 has spring nature is large, and it is shown that it can change into an open condition more certainly than the case where it is the operation gestalt 1.
[0014] The resistance after penetration destruction of the chip mold varistor in this operation gestalt 2 and the resistance after penetration destruction of the chip mold varistor of the conventional example are shown in (a table 1). this (table 1) -- from -- when the chip mold varistor by the operation gestalt 2 gives spring nature to lead terminal 33b to be used shows that the failure mode of a chip mold varistor can be more certainly changed into an open condition after penetration destruction of the ceramic varistor component 31 so that clearly.
[0015]
[Effect of the Invention] As mentioned above, offer of the chip mold varistor which opens this invention certainly at the time of failure is attained.

[Translation done.]

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TECHNICAL FIELD

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PRIOR ART

[Description of the Prior Art] In drawing 15 and drawing 16 , 11 is a varistor component. They are a lead terminal and the electroconductive glue with which the electrode which prepared 12a and 12b in the principal plane of the varistor component 11, and 13a and 13b connect 14a, and 14b connects lead terminals 13a and 13b with Electrodes 12a and 12b. 15 is mould resin. About the chip mold varistor constituted as mentioned above, the actuation is explained below.
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EFFECT OF THE INVENTION

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] With the aforementioned conventional configuration, when it is covered with mould resin 15 and the varistor component 11 carries out penetration destruction, the high pressure gas which occurs in connection with it destroys mould resin 15, and the flow of the varistor component 11 and lead terminals 13a and 13b is severed. However, it had the problem that there was a possibility that the varistor component 11 may not be in an open condition depending on the part where mould resin 15 is destroyed.
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MEANS

[Means for Solving the Problem] In order to attain this object, the chip mold varistor of this invention establishes a slot in the up front face of the mould resin in alignment with a lead terminal periphery, and, thereby, attains the early object.

[0007]
[Embodiment of the Invention] According to invention of this invention according to claim 1, it becomes weaker than a part without the mechanical-strength fang furrow of the part of the slot established in the up front face of mould resin. Therefore, when a varistor component causes penetration destruction, it is sheared from the part of a slot with the pressure of the gas which occurred, and the mould resin on the top face of a lead terminal exfoliates with a lead terminal so that a lid may open. For this reason, it will be in an open condition electrically between an electrode and a lead terminal.
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[0010]
[A table 1]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The plan of the chip mold varistor by the operation gestalt 1 of this invention
[Drawing 2] Top-face perspective drawing of the chip mold varistor by this operation gestalt 1
[Drawing 3] The A-A sectional view of drawing 1
[Drawing 4] The plan showing the destructive condition of the chip mold varistor by this operation gestalt 1
[Drawing 5] The A-A sectional view of drawing 4
[Drawing 6] The plan of the lead terminal by this operation gestalt 1
[Drawing 7] The side elevation of the lead terminal by this operation gestalt 1
[Drawing 8] The plan of the chip mold varistor by the operation gestalt 2 of this invention
[Drawing 9] Top-face perspective drawing of the chip mold varistor by this operation gestalt 2
[Drawing 10] The A-A sectional view of drawing 8
[Drawing 11] The plan showing the destructive condition of the chip mold varistor by this operation gestalt 2
[Drawing 12] The A-A sectional view of drawing 11
[Drawing 13] The plan of the lead terminal by this operation gestalt 2
[Drawing 14] The side elevation of the lead terminal by this operation gestalt 2
[Drawing 15] Top-face perspective drawing of the chip mold varistor of the conventional example
[Drawing 16] The A-A sectional view of drawing 15
[Description of Notations]
21 Ceramic Varistor Component
22 Electrode
23b Lead terminal
25 Mould Resin
26 Slot

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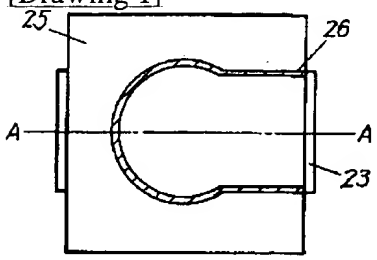
DRAWINGS

[Drawing 1]



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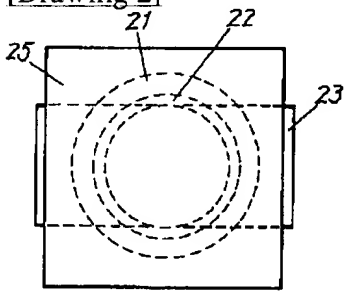

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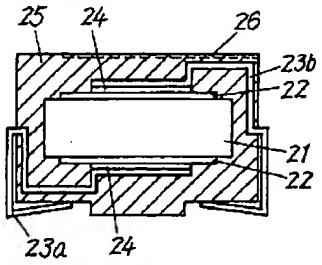
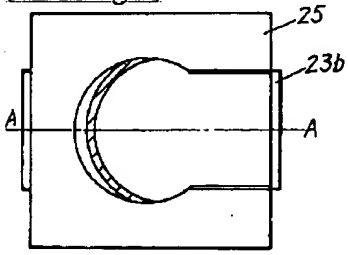


21 セラミック
バリスタ素子
23b リード端子
25 モールド樹脂
26 溝

[Drawing 4]



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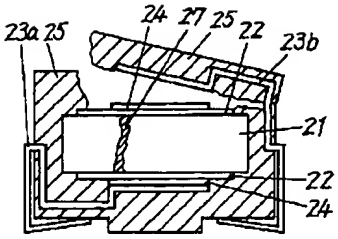

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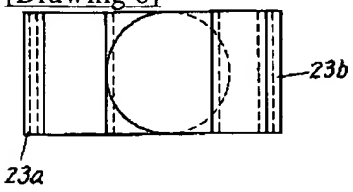

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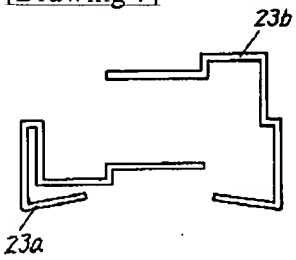

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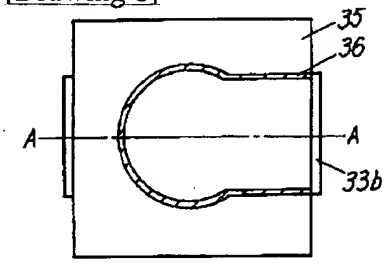

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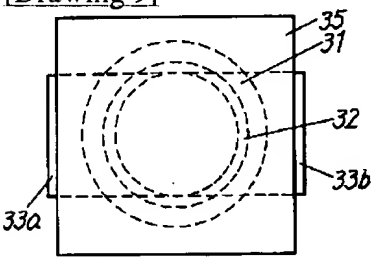

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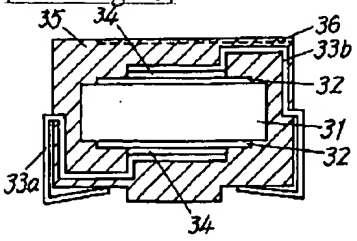

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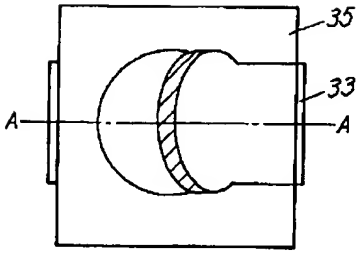
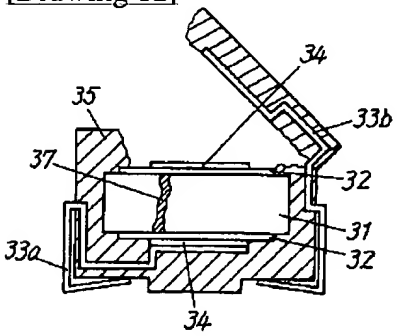


[Drawing 12]



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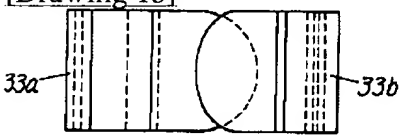
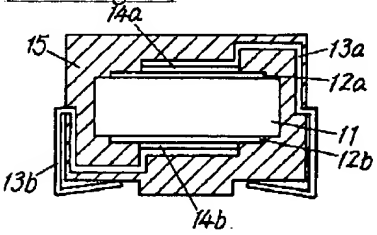
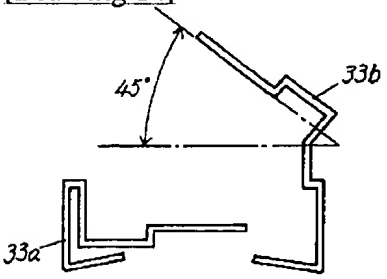


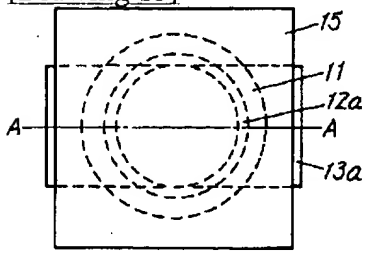
[Drawing 16]



[Drawing 14]



[Drawing 15]



[Translation done.]

引用例 2

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号

特開平9－129404

(43)公開日　平成９年(1997)５月16日

(51)Int.Cl.⁶		識別記号	庁内整理番号	ＦＩ			技術表示箇所
Ｈ０１Ｃ	1/14			Ｈ０１Ｃ	1/14	Ｚ	
	1/02				1/02	Ｚ	
	7/10				7/10		

審査請求　未請求　請求項の数２　ＯＬ　（全５頁）

(21)出願番号　特願平7－278801

(22)出願日　平成７年(1995)10月26日

(71)出願人　000005821
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(72)発明者　中村　和幸
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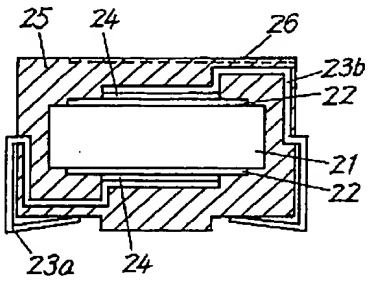
(54)【発明の名称】　チップ型バリスタ

(57)【要約】

【課題】　セラミックバリスタ素子の貫通破壊時に確実に開放するようにすることを目的とする。

【解決手段】　セラミックバリスタ素子２１を覆ったモールド樹脂２５の上部表面にリード端子２３ｂの外周に沿って溝２６を設けた。



21　セラミックバリスタ素子
23b　リード端子
25　モールド樹脂
26　溝

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【特許請求の範囲】

【請求項１】　バリスタ素子と、この主平面に設けた電極と、前記電極に電気的に接続したリード端子と、前記バリスタ素子と電極およびリード端子の少なくとも電極との接続部を覆った樹脂モールドとを備え、前記リード端子外周に沿ってモールド樹脂の上部表面に溝を設けたことを特徴とするチップ型バリスタ。

【請求項２】　リード端子には、バネ性を持たせた請求項１記載のチップ型バリスタ。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明はテレビジョン受像機、洗濯機、自動車電装装置などの電源回路に生じるサージ電圧を吸収する異常電圧対策に用いるチップ型バリスタに関するものである。

【０００２】

【従来の技術】図１５、図１６において、１１はバリスタ素子である。１２ａ，１２ｂはバリスタ素子１１の主平面に設けた電極、１３ａ，１３ｂはリード端子、１４ａ，１４ｂは電極１２ａ，１２ｂとリード端子１３ａ，１３ｂを接続する導電性接着剤である。１５はモールド樹脂である。以上のように構成されたチップ型バリスタについて、以下その動作について説明する。

【０００３】まず、バリスタ素子１１自身が耐え得ないような異常高電圧が負荷された場合、バリスタ素子１１が貫通破壊を起こす。

【０００４】

【発明が解決しようとする課題】前記の従来の構成ではモールド樹脂１５によって覆われており、バリスタ素子１１が貫通破壊した際に、それに伴って発生する高圧ガスがモールド樹脂１５を破壊し、バリスタ素子１１とリード端子１３ａ，１３ｂの導通を断つ。しかしモールド樹脂１５の破壊される箇所によっては、バリスタ素子１１が開放状態にならないおそれがあるという問題を有していた。

【０００５】本発明は従来の課題を解決するもので、バリスタ素子１１が貫通破壊した場合、確実に開放状態となるようにすることを目的とする。

【０００６】

【課題を解決するための手段】この目的を達成するため40に本発明のチップ型バリスタは、リード端子外周に沿ったモールド樹脂の上部表面に溝を設け、これにより初期の目的を達成するものである。

【０００７】

【発明の実施の形態】本発明の請求項１に記載の発明によれば、モールド樹脂の上部表面に設けた溝の部分の機械的強度が溝の無い部分より弱くなる。したがってバリスタ素子が貫通破壊を起こした場合、発生したガスの圧力により溝の部分よりせん断され、リード端子と共にリード端子上面のモールド樹脂が蓋が開くように剥離する。このため電極とリード端子間は電気的に開放状態となる。

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【０００８】（実施形態１）図１は本発明の実施例におけるチップ型バリスタの上面図、図２は上面透視図、図３は図１のＡ－Ａ断面図を示すものである。図３において、２１は酸化亜鉛系のセラミックバリスタ素子である。２２はセラミックバリスタ素子２１の主平面に設けた電極、２３ａ，２３ｂはリード端子である。２４は電極２２とリード端子２３ａ，２３ｂを電気的に接続する導電性接着剤である。２５はバリスタ全体を覆ったエポキシ絶縁樹脂よりなるモールド樹脂、２６はリード端子２３ｂ外周に沿ってモールド樹脂２５の上部表面に設けられた溝である。以上のように構成されたバリスタの動作について図を用いて説明する。

【０００９】セラミックバリスタ素子２１は定常状態では良好な絶縁体であるが、セラミックバリスタ素子２１自身が耐え得ないような異常高電圧が印加されると、セラミックバリスタ素子２１が貫通破壊をおこす。この際、破壊したセラミックバリスタ素子２１が高温になり、組成の一部が蒸発する。これに伴って高温、高圧のガスが発生する。このガスの圧力はモールド樹脂２５を破壊するように働き機械的強度の弱い溝２６の部分に沿って亀裂を生じ、せん断させ、そのガスの圧力によりリード端子２３ｂと共にセラミックバリスタ素子２１上面のモールド樹脂２５が、蓋が開くように剥離し、電気的に開放状態となる。図４、図５に本実施形態におけるリード端子２３ｂと共に、上面のモールド樹脂２５が蓋が開くように剥離した状態を示す。図６に本実施例に用いたリード端子２３ａ，２３ｂの上面図、図７に同じく側面図を示す。本実施例におけるチップ型バリスタの貫通破壊後の抵抗値と従来例のチップ型バリスタの貫通破壊後の抵抗値を（表１）に比較して示している。なおセラミックバリスタ素子２１には最大許容電圧の２倍の電圧を印加し過電圧破壊を起こさせたものである。

【００１０】

【表１】

破壊後の端子間抵抗値Ω　n＝10		
従来品	実施形態１品	実施形態２品
22	300000以上	300000以上
73	2927	300000以上
209	300000以上	300000以上
3582	300000以上	300000以上
3	300000以上	300000以上
24	52000	300000以上
16	300000以上	300000以上
229	375	300000以上
2	526	300000以上
146	300000以上	300000以上

※抵抗測定器の測定範囲 300000Ω Max.

【００１１】この（表１）から明らかなように、本発明によるチップ型バリスタは破壊後の抵抗値が開放状態になる事がわかる。以上のように本実施形態は、リード端子２３ｂの外周に沿ってモールド樹脂２５の上部表面に溝２６を設けたものであり、セラミックバリスタ素子２１が貫通破壊した際のチップ型バリスタの故障モードを開放状態にすることができる。

【００１２】（実施形態２）図８～図１０において、３１はセラミックバリスタ素子、３２は電極、３３ａ，３３ｂはリード端子、３４は導電性接着剤、３５はモールド樹脂、３６はモールド樹脂３５の上部表面の溝であり、実施形態１と同様な構成である。実施形態１と異なるのは、リード端子３３ｂにセラミックバリスタ素子３１が貫通破壊したときに離れやすいようにバネ性を持たせた点である。図１３に本実施例に用いたリード端子３３ａ，３３ｂの上面図、図１４に同じく側面図を示した。本実施例に用いたリード端子３３ｂの途中より４５°の角度に曲げ加工しているので、これをセラミックバリスタ素子３１側へ押圧してモールド樹脂３５で覆うとバネ性が発揮される。図１１、図１２は本実施形態における、セラミックバリスタ素子３１が貫通破壊したとき、リード端子３３ｂと共に、セラミックバリスタ素子３１電極３２上面のモールド樹脂３５が溝３６に沿って蓋が開くように剥離した状態図を示す。

【００１３】以上のように構成されたチップ型バリスタ40の動作について、図を用いて説明する。セラミックバリスタ素子３１の貫通破壊で、リード端子３３ｂがモールド樹脂３５をせん断するまでのプロセスは、実施形態１と同様であるが本実施形態２に用いているリード端子＊

＊３ｂはバネ性を持っているため、ガスの圧力により剥離したリード端子３３ｂの開く角度が大きく、実施形態１の場合より、より確実に開放状態にすることができることを示している。

【００１４】本実施形態２におけるチップ型バリスタの貫通破壊後の抵抗値と、従来例のチップ型バリスタの貫通破壊後の抵抗値を（表１）に示している。この（表１）から明らかなように、実施形態２によるチップ型バリスタは、使用するリード端子３３ｂにばね性をもたせることによりセラミックバリスタ素子３１の貫通破壊後、チップ型バリスタの故障モードをより確実に開放状態にすることができることが分かる。

【００１５】

【発明の効果】以上のように、本発明は故障時に確実に開放するチップ型バリスタの提供が可能になる。

【図面の簡単な説明】

【図１】本発明の実施形態１によるチップ型バリスタの上面図

【図２】同実施形態１によるチップ型バリスタの上面透視図

【図３】図１のＡ－Ａ断面図

【図４】同実施形態１によるチップ型バリスタの破壊状態を示す上面図

【図５】図４のＡ－Ａ断面図

【図６】同実施形態１によるリード端子の上面図

【図７】同実施形態１によるリード端子の側面図

【図８】本発明の実施形態２によるチップ型バリスタの上面図

【図９】同実施形態２によるチップ型バリスタの上面透視図

【図１０】図８のＡ－Ａ断面図

【図１１】同実施形態２によるチップ型バリスタの破壊状態を示す上面図

【図１２】図１１のＡ－Ａ断面図

【図１３】同実施形態２によるリード端子の上面図

【図１４】同実施形態２によるリード端子の側面図

【図１５】従来例のチップ型バリスタの上面透視図

【図１６】図１５のＡ－Ａ断面図

【符号の説明】

２１　セラミックバリスタ素子

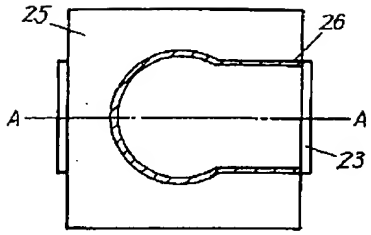
２２　電極

２３ｂ　リード端子

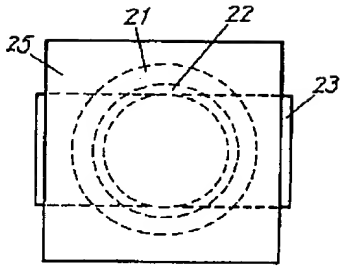
２５　モールド樹脂

２６　溝

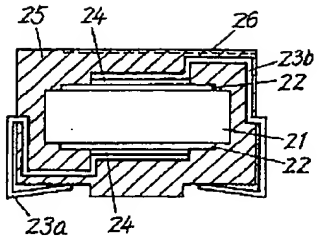
【図１】



【図２】

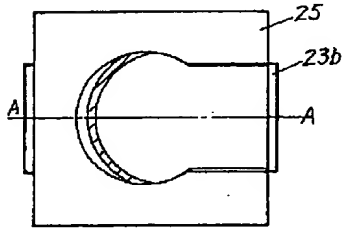


【図３】

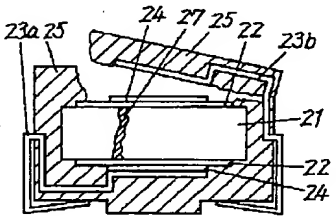


21 セラミック
バリスタ素子
23b リード端子
25 モールド樹脂
26 溝

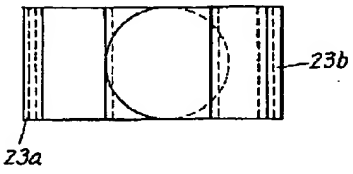
【図４】



【図５】



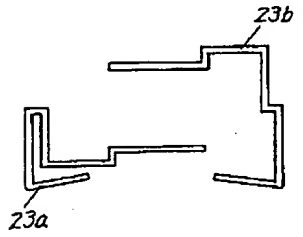
【図６】

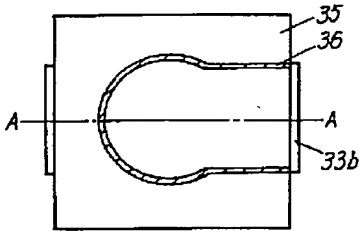


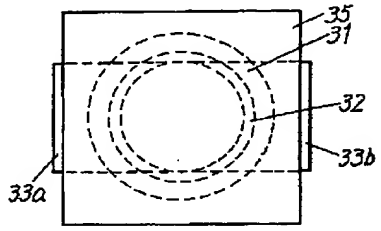
【図７】

【図８】

【図９】



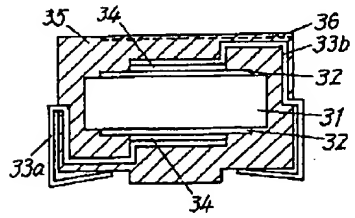


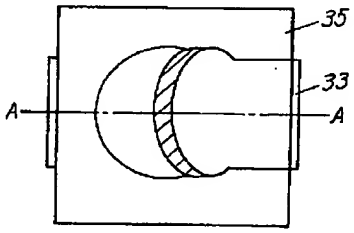


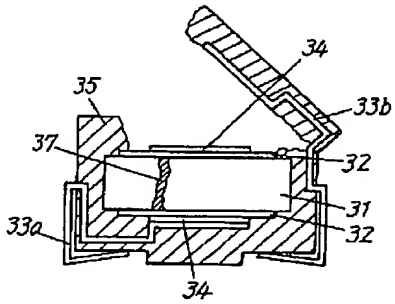
【図１０】

【図１１】

【図１２】

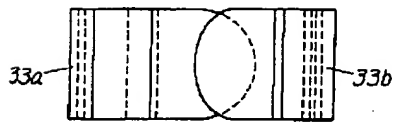


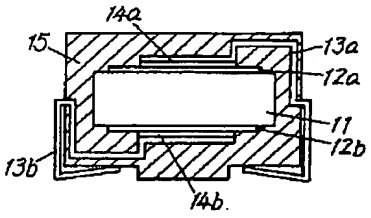




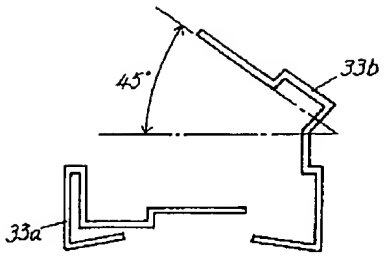
【図１３】

【図１６】





【図１４】



【図１５】